Döcket No.: 57810-093

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277

Hideaki FUJIWARA, et al. : Confirmation Number:

Serial No.: : Group Art Unit:

Filed: March 23, 2004 : Examiner: Unknown

For: SEMICONDUCTOR DEVICE INCLUDING FIELD-EFFECT TRANSISTOR

INFORMATION DISCLOSURE STATEMENT

Mail Stop IDS Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The relevance of the article, "Transistor Elements for 30nm Physical Gate Length and Beyond" is discussed in the present specification.

Serial No.:

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

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Date: March 23, 2004

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		Bri	ian DOYLE, et al. "Transis	tor Elements for 3 Issue	Onm Physical Gate Lengths and E 2, May 16, 2002, ISSN 1535766X	Physical Gate Lengths and Beyond", Intel Technology Journal, Vol. 6, lay 16, 2002, ISSN 1535766X				
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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.